MICROELECTRONIC CIRCUITS

ASSIGNMENT - 2

GROUP - 162

SET - 3

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Question 1

CSA Amplifier

Required Specifications

(i) Voltage Gain = 70 ± 5% dB

(ii) 3dB frequency = 60k ± 5% rad/s

(iii) Power Dissipation = 2 ± 5% mW

Question 2

Emitter follower

Required Specifications

(i) Current Gain = 85 ± 5% dB

(ii) 3dB frequency = 60k ± 5% rad/s

(iii) Power Dissipation = 2 ± 5% mW

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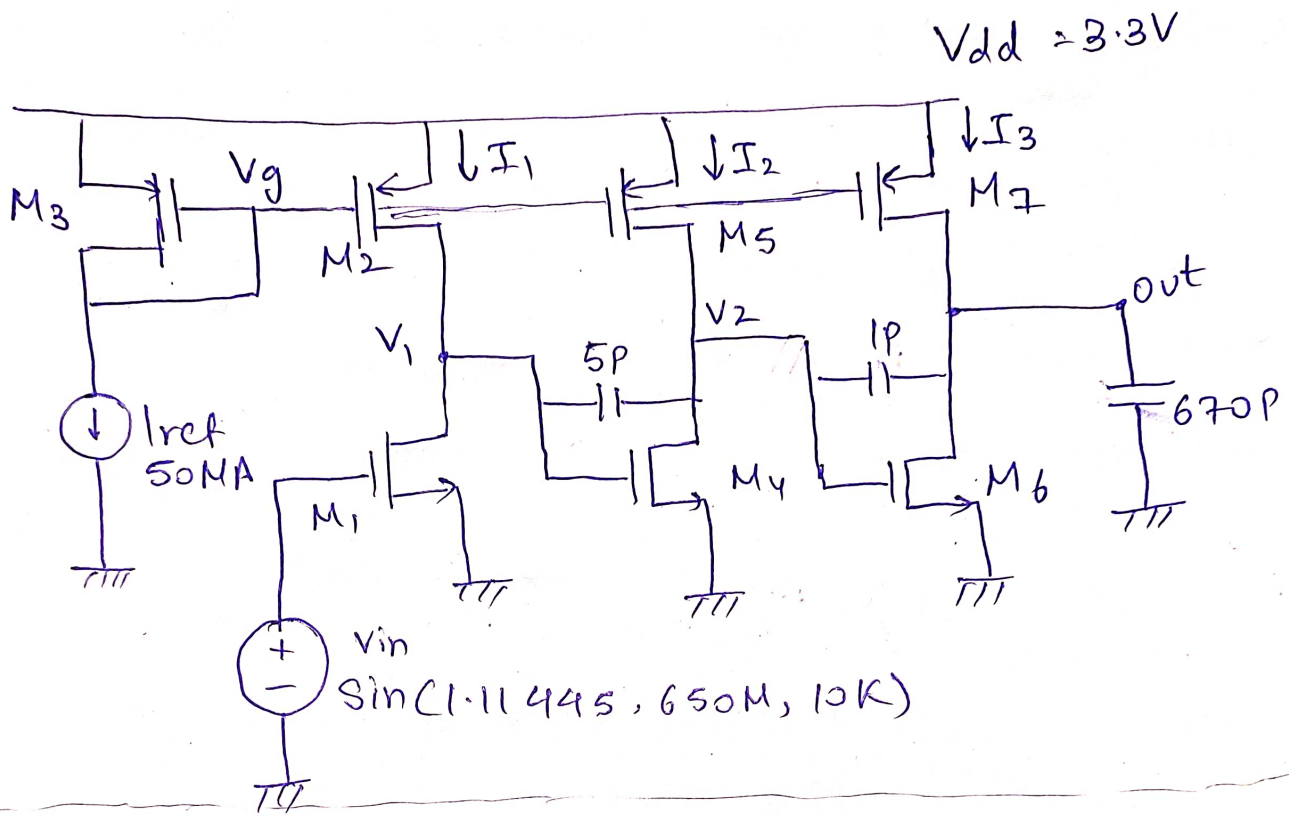
CIRCUIT



DC operating point

$V_g = 1.617\,V = V_{g2} = V_{g5} = V_{g7}$

$V_1 = 1.116\,V = V_{g4}$

$V_2 = 1.089\,V = V_{g6}$

$V_{out} = 1.566\,V$

$V_{g1} = 1.11445\,V$

$I_2 = 190.45\,MA$

$I_1 = 190.015\,MA$

$I_3 = 181.9\,MA$

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CIRCUIT DESCRIPTION

The circuit designed is most common design for a Common Source Amplifier One current mirror arm ~~and other~~ to get perfect / or desired bias in the Amplifier MOSFET. Three stages have been cascaded for the purpose of increment of gain, which was quite high, around 70dB.

All MOSFETS work in saturation region as clear through the DC operating point. The load capacitor's value is increased to a high value to get desired bandwidth.

Also some (2) capacitors (Cgd) were added before 2 stages for the improvement in phase plot of the Amplifier.

The calculations, Results, $\frac{W}{L}$ values are shown. Also changes made and extra additions to circuit are also listed towards end.

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Power consumption $\approx$ 2mW (acc. to spec)

So $3.3 \times I_{Total} = 2mW$

$\Rightarrow 3.3 \times (50M + I_1 + I_2 + I_3) = 2mW$

$\Rightarrow I_1 + I_2 + I_3 = 556.06MA$

So if we take them all equal we get $I_1 = I_2 = I_3 = 185.35MA$

Now for first (amplifier) arm

V_{SG} is same as V_{SG} of pmos(M) in Reference arm.

and V_D of $M2$ = V_{DS} of $M1$

and $V_{DS}(M_1) > V_{GS_{M_1}} - V_t$

$V_{DS} > 1.114 - 0.67$

$\Rightarrow V_D > 0.44V$

$\Rightarrow V_{SD} < 2.856V$

also $V_{SD} > V_{SG} - 0.9214$

OR $V_D < V_{G(PMOS)} + 0.9214$

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for M7 arm

$$50 = \frac{1}{2} K_p \left(\frac{W}{L}\right) V_{ov}^2 (1+\lambda V_{SD})$$

$$100 = K_p \left(\frac{W}{L}\right)_7 V_{ov}^2 (1+\lambda V_{SD_7}) \quad -(1)$$

for (M_2, M_1 arm) (1st amp arm)

$$185.35 = \frac{K_p}{2} \left(\frac{W}{L}\right)_2 V_{ov}^2 (1+\lambda V_{SD_2}) \quad -(2)$$

[V_{ov} is same for both as V_G is same]

Taking $\lambda \approx 0$

we get (Divide) (2) by (1)

$$3.7 = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_7}$$

Taking $\left(\frac{W}{L}\right)_7 \approx 5$

So $\left(\frac{W}{L}\right)_2 = 18.5$

$\Rightarrow \left(\frac{W}{L}\right)_1 \approx 18.5$ only to allow current I_D to flow

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Similarly for the other amplifier arms

$$\left(\frac{W}{L}\right)_{M5} : \left(\frac{W}{L}\right)_{M7} = 18.5$$

$$\left(\frac{W}{L}\right)_{M4} : \left(\frac{W}{L}\right)_{M6} = 18.5$$

TABLE of $\frac{W}{L}$ calculations vs Simulation $\left(\frac{W}{L}\right)$.

MOSFET	Hand Calc.	Simulation
M_1	18.5	15
M_2	18.5	15
M_3	5	5
M_4	18.5	15
M_5	18.5	15
M_6	18.5	15
M_7	18.5	15

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Specifications

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SPECIFICATIONS AND RESULTS TABLE

	Specs	Required	Simulation
1.	Voltage Gain	66.5 – 73.5 dB	71.95 dB
2.	3dB Bandwidth	9.07 – 10.026 KHz	9.77 kHz
3.	Power Dissipation	1.9 – 2.1 mW	1.97 mW
4.	Output Swing	2.64 V (atleast)	2.66 V
5.	Phase margin	atleast 45°	176.25°
6.	Power rails	3.3V & gnd	3.3V & gnd
7.	Current Source	50MA (1)	50MA (1)
8.	ICMR	0.66 – 2.64V	1.112 – 1.116 V
9.	Gain margin		59.08 dB
10.	Rin		38.06 MΩ
11.	Rout		60 KΩ

EXTRA CHANGES DONE

1. Cload (C_2) we increased to 670pF from 1pF to reduce to 3dB bandwidth to required (desired value).

2. C_1 and C_3 were added in model for phase plot. ~~and also made the model~~ stable. Since Cgd plays an imp. role in poles/zeros and Amplitude/Phase plots. They made the phase more clearer and real. It was coming positive (the whole phase plot) without C_1 & C_3.

SPICE NETLIST

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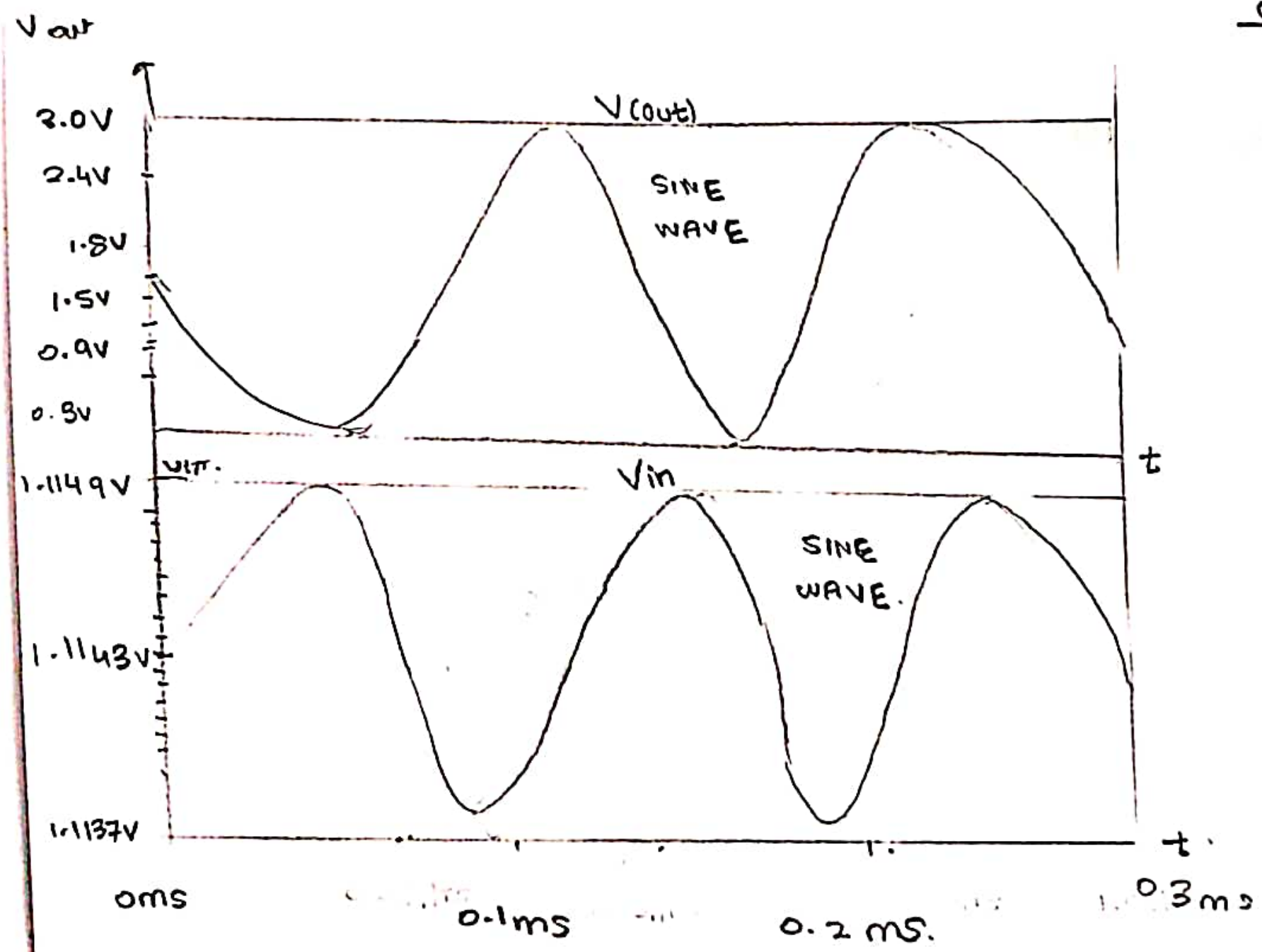
```
M1   1   Vin  0   0   NMOS  l=600n w=9u
M2   Vdd Vg   1   Vdd PMOS  l=600n w=9u
M3   Vdd Vg   Vg  Vdd PMOS  l=600n w=3u
I1   Vg  0    50u
V1   Vdd 0    3.3
V2   Vin 0    Sine(1.1145 650u 10K) AC 650u
M4   2   1    0   0   NMOS  l=600n w=9u
M5   Vdd Vg   2   Vdd PMOS  l=600n w=9u
M6   out 2    0   0   NMOS  l=600n w=9u
M7   Vdd Vg   out Vdd PMOS  l=600n w=9u
C2   out 0    670p
C1   2   out  1p
C3   1   2    5p
.model NMOS NMOS
.model PMOS PMOS
.op
.ac dec 100 1 1G
.dc V2 0 5 0.00009
tran 1n
.backanno
.end
```



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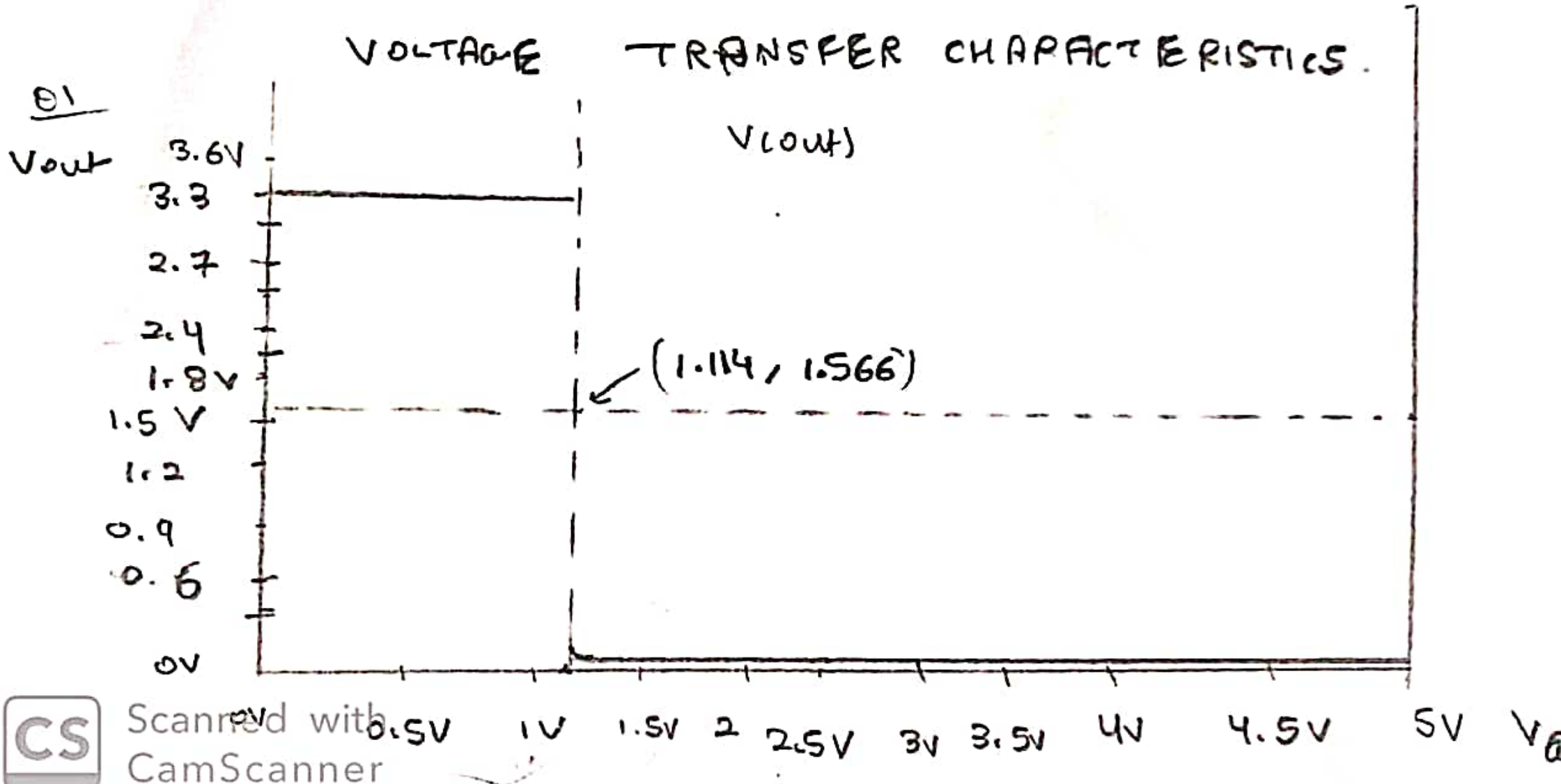

FREQUENCY RESPONSE.

mag - 68.96 dB

freq - 9.772 Hz

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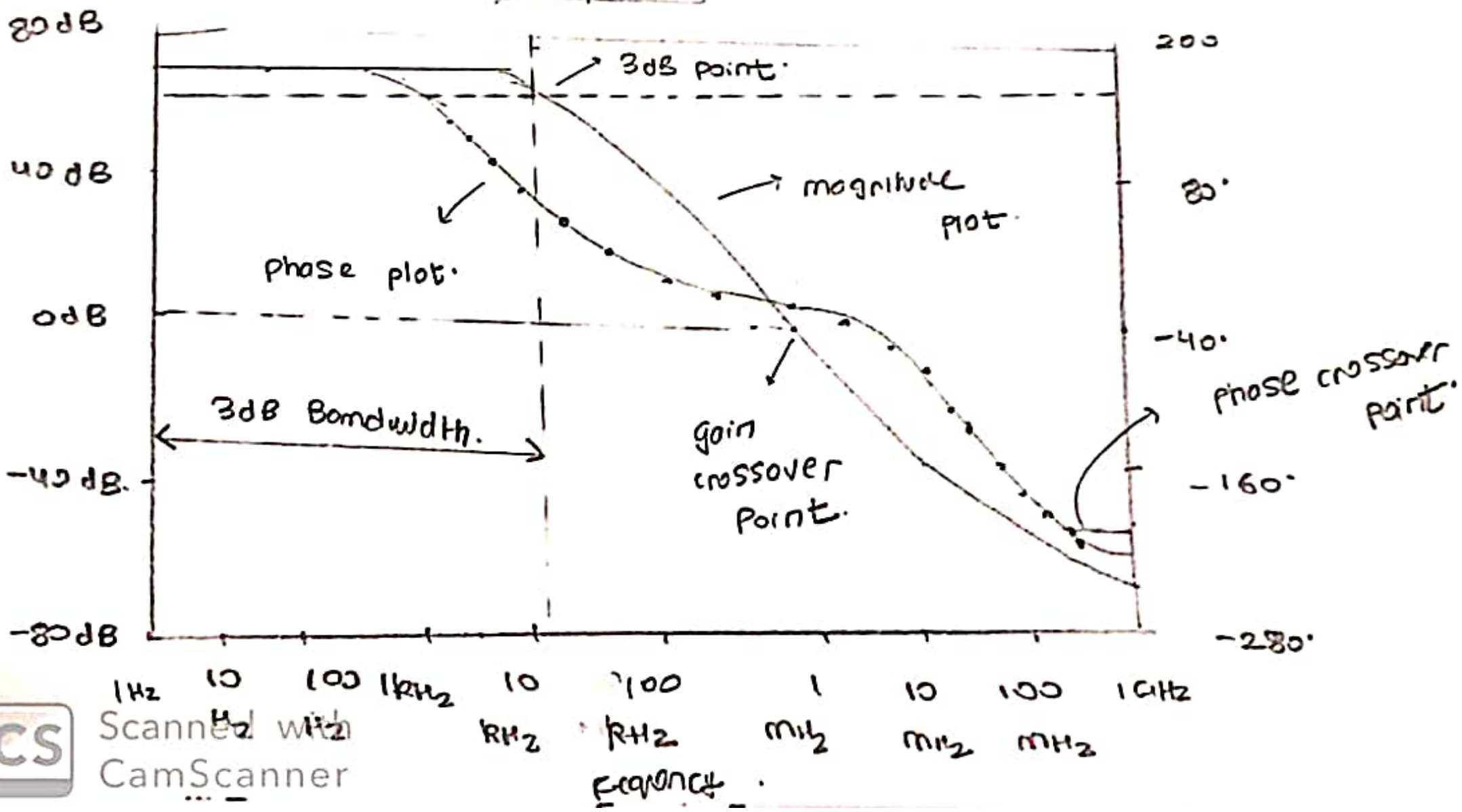

Question 2

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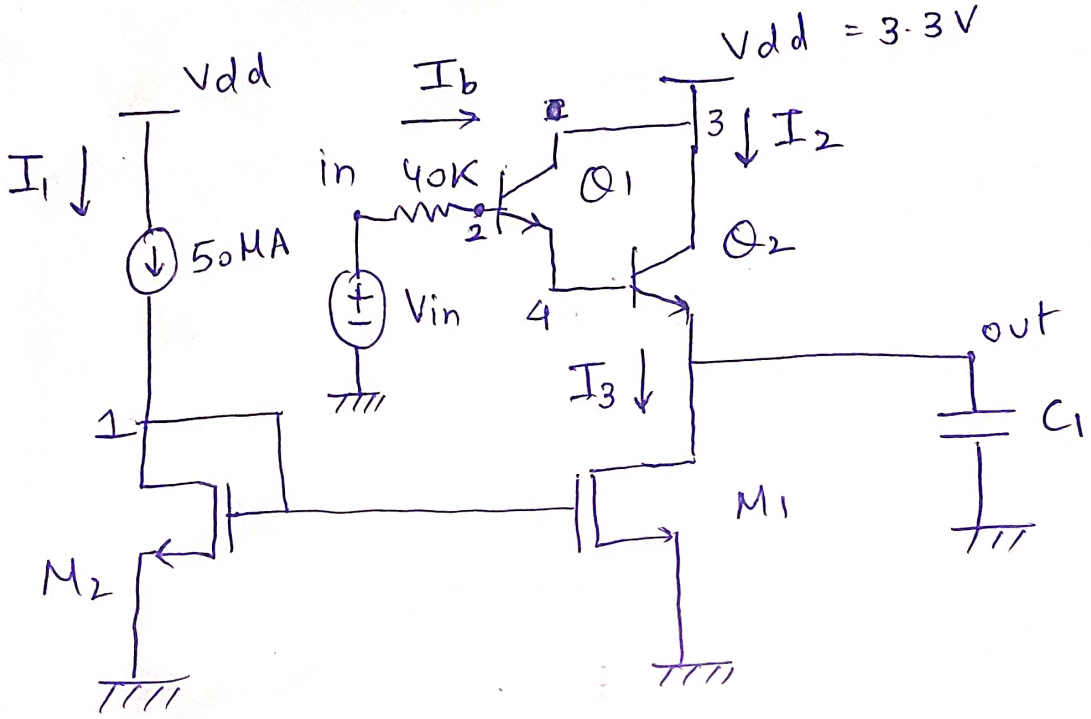
Circuit



DC operating point

Vin = 2.5V

$I_b = 2.76 \times 10^{-2}$ MA

I_1 = 50MA

I_2 = 530.519 MA

I_3 = 532.704 MA

Vout = 1.34665V

V_4 = 1.99386V

V_1 = 1.2 V

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CIRCUIT DESCRIPTION

The topology used here is MOSFET current mirror to get desired current in the arm of emitter follower. The emitter follower has been chosen as Darlington pair because of high current, specifications. gain.

Calculations of $\frac{W}{L}$ of both MOSFETS is shown and the Table of specifications required and specifications achieved is also drawn. Along with the Tradeoffs and changes done to the circuit are mentioned.

$I_1 = 50\,mA$

$$I_1 = \frac{K_n}{2}\left(\frac{W}{L}\right)_2 V_{ov}^2 (1+\lambda V_{DS})$$

$$I_3 = \frac{K_n}{2}\left(\frac{W}{L}\right)_1 V_{ov}^2 (1+\lambda V_{DS_2})$$

Supposing λ to be very small

we get $$\frac{I_1}{I_3} = \frac{(W/L)_2}{(W/L)_1}$$

Now using power consumption constraint

we get $I_3 = 556.06\,mA$

$$\Rightarrow \frac{(W/L)_2}{(W/L)_1} = \frac{50}{556.06}$$

$$\text{So } \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 \times \frac{556.06}{50}$$

$$\left(\frac{W}{L_1}\right) = 11.12\left(\frac{W}{L}\right)_2$$

Take $\left(\frac{W}{L}\right)_2 = 5$ so $\left(\frac{W}{L}\right)_1 = 55.6$

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	Spice Values of $(\frac{W}{L})$	Calculated Values
M_1	28.33	55.6
M_2	5	5

SPECIFICATIONS TABLE

	Specs	Required	Achieved (Sim)
1.	Current Gain	80.75 - 89.25 dB	86.67 dB
2.	Power Consumption	1.9 - 2.1 mW	1.923 mW
3.	3dB Bandwidth	9K - 10KHz	9.77KHz
4.	Phase margin	45°	≈ 180°
5.	Gain margin		55dB
6.	ICMR	0.66 - 2.64V	0.8 - 3.3V
7	Output Swing	2.64V	[0.2V] *
8	Iref	50 MA	50MA
9	Voltage rail	3.3V - gnd	3.3V - gnd
10.	Rin		25MΩ
11.	Rout		20kΩ

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TRADE-OFFS AND SOME CHANGES

1- ~~Since~~ The capacitor value required to be 1pF. That is changed to a considerably high value, i.e. 180nF to achieve the desired 3dB band width.

Now changing capacitor value posed a Trade off :- The output voltage swing reduced considerably from around 2.6V (as it was in case when C_{load} = 1pF) to 0.2V.

⇒ Since we had to chose ~~betw~~ 1 b/w 2 of the specifications we decided to go for the 3dB band width and increased the capacitor value to 180nF.

⇒ Had we gone for 1pF capacitance at load, then 3dB BW came out to be in MegaHertz which is much much higher than 10KHz. But in that case our output swing would be just fine.

SPICE NETLIST

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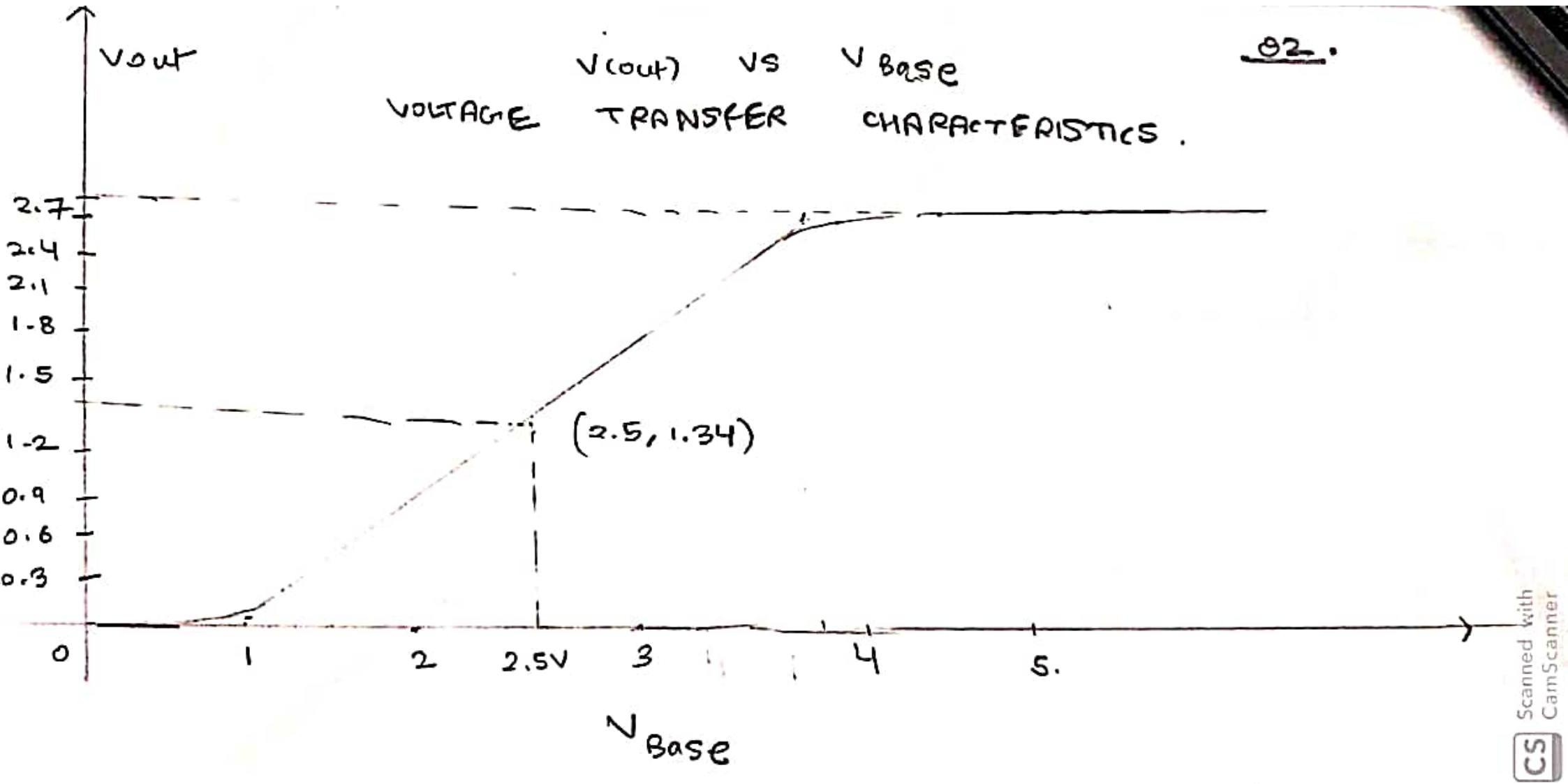
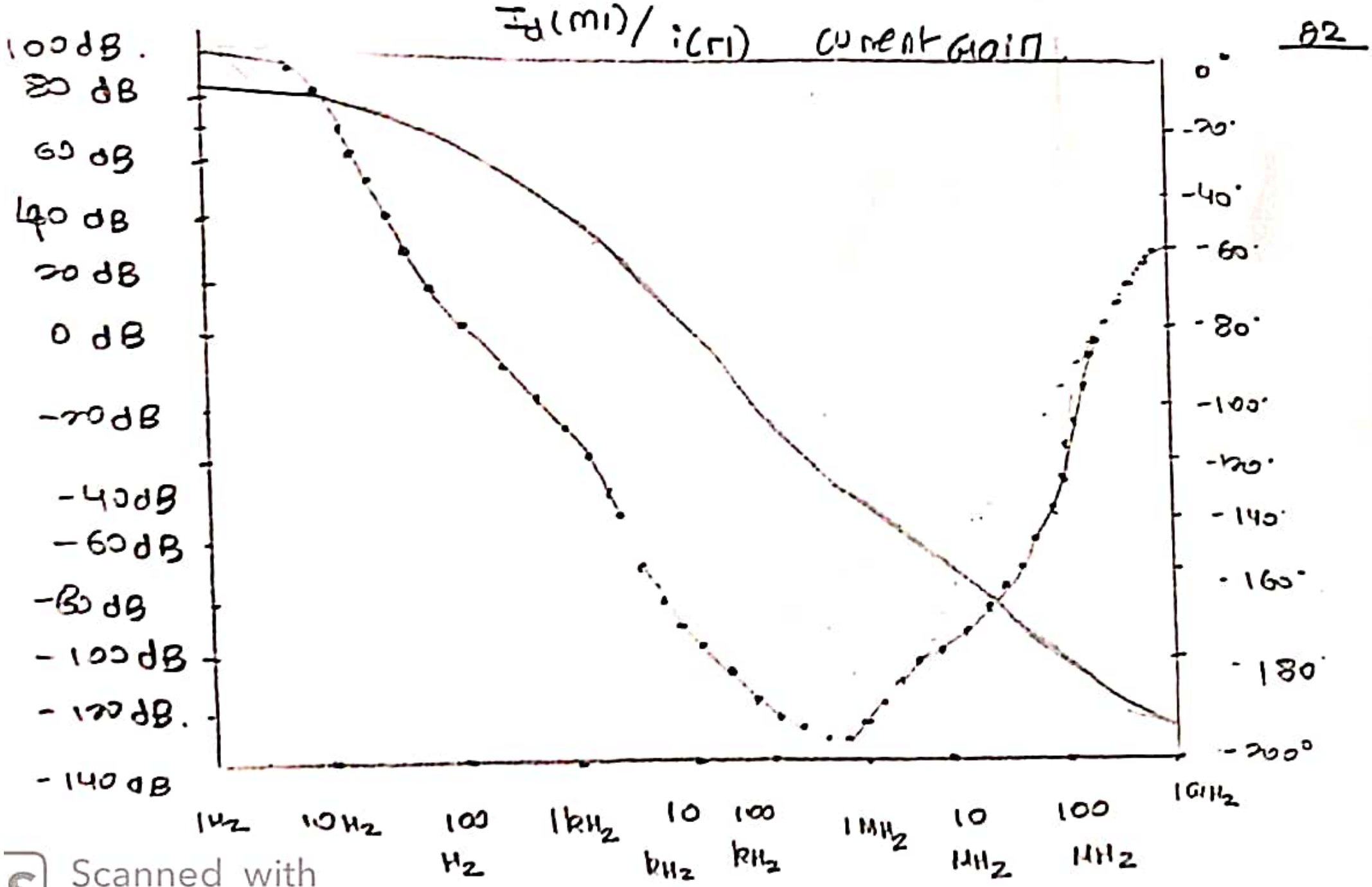
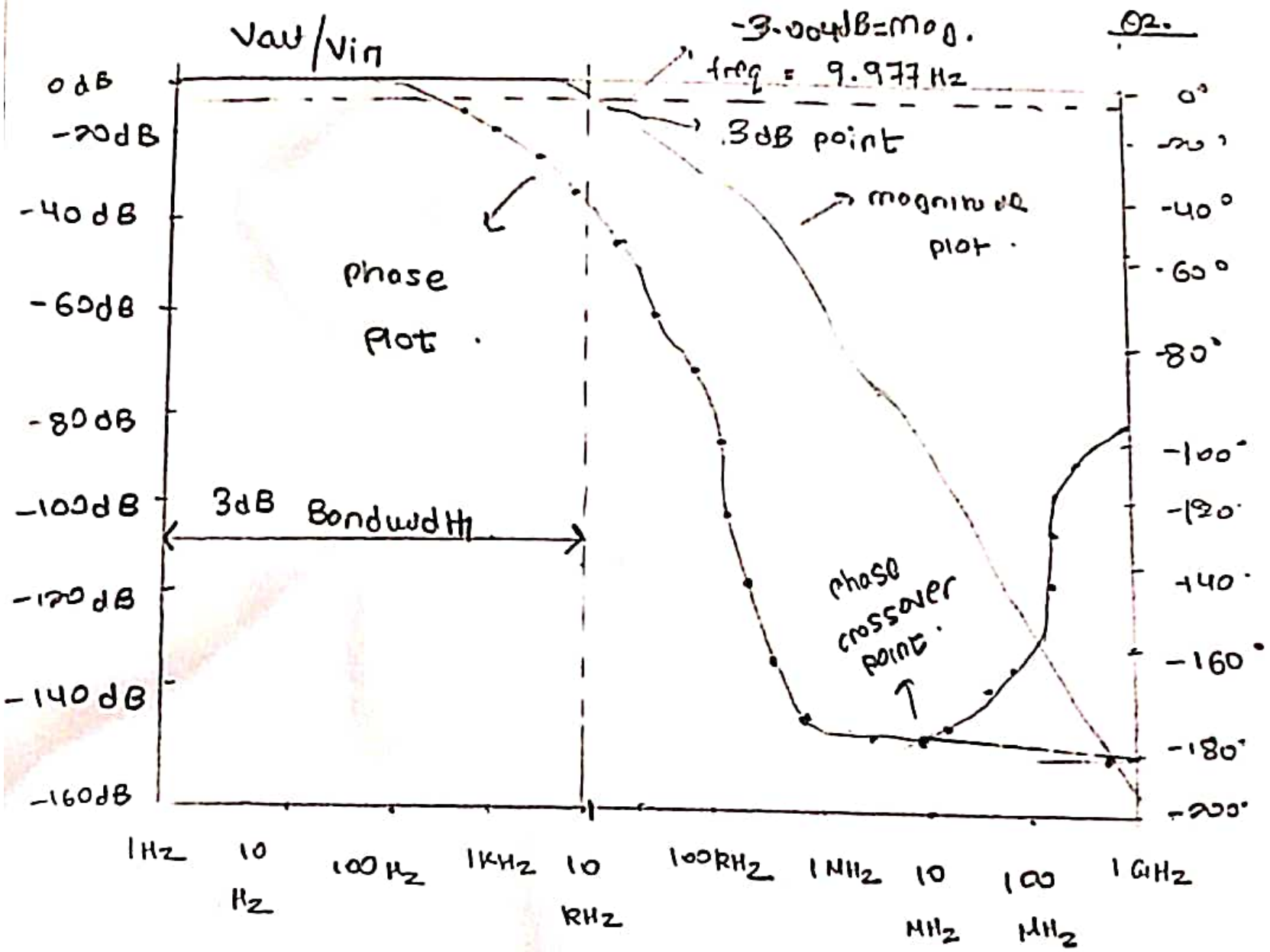
```
Vdd    3    0    3.3
Q2     3    4    out   0    BC107B
C2     out  0    180n
Q1     3    2    4     0    BC107B
Vin    in   0    SINE (2.5 1.4 10K) AC 1.4
I1     3    1    50µ
M1     out  1    0     0    NMOS L=600n W=17M
M2     1    1    0     0    NMOS L=600n W=3µ
R1     in   2    40K
.model NPN  NPN
.model PNP  PNP
;dc Vin 0 3.3 0.01
;ac dec 100 1 1G
;op
;tran 1m
.model BC107B NPN( - - - )
.model NMOS NMOS( - - - - )
.backanno
.end.
```

V(out) VS V Base

VOLTAGE TRANSFER CHARACTERISTICS.







Frequency Response